International Journal of Computer Information Systems and Industrial Management Applications.
ISSN 2150-7988 Volume 6 (2014) pp. 355 - 363

Delay Modelling of On-Chip RC Global VLSI Interconnect for Step Input

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Abstract— **This paper presents an accurate and efficient model to compute the delay metric of on chip high speed VLSI interconnects. The proposed delay metric assumption is based on RC interconnect model. Interconnect has become a dominant factor in deep sub micrometer (DSM) integrated circuit (IC) technology. The Elmore delay has been the metric of choice for the performance driven design applications. But the accuracy of the Elmore delay is insufficient. For optimization like physical synthesis and static timing analysis, efficient interconnect delay computation is critical. In this paper, a delay metric using RC-int and RC-out has been formulated which computes the delay at any arbitrary point on the waveform and at any point along the interconnect line. The proposed model is based on the first three moments of the impulse response. Two pole RC model is developed based on the first, second and third moments' effect onto the delay calculation for interconnect lines. This two pole approach permits the pre-characterization of the interconnect delay. The empirical D3M metric is shown to be a special case one present here, the accuracy of delay metric is insufficient, the metric also provides an expression for impulse response, we absorbs significant improvement of at least 50% accuracy delay estimate when compared to the Elmore delay and even through our estimate are as ease to compute as Elmore delay, the metric has proven to be accurate to with in 50% of HSPICE simulation. The proposed metric also provides an expression for impulse response. The SPICE simulation results justify the accuracy and efficiency of the proposed model. . The novelty of the work is that it does not require any look-up table for the calculation of the delay.**

Keywords **-** Delay Modelling, On-Chip Interconnect, RC Line, Step Input, VLSI.

I. Introduction

The developments in VLSI process technology using nanometres-scale components focus on the speed estimations from transistors and gates to interconnect. As CMOS technologies shift towards deep sub-micron (DSM) technologies, interconnect networks are becoming increasingly dominant in terms of total path delay [1]. The model order reduction techniques [2] compute the dominant poles and the corresponding residues by matching the moments of the circuit impulse response. The design optimization of digital integrated circuits requires millions of delay calculations. During early designing the design optimization stages are efficient and implemented easily, in that time high accuracy is not required, therefore delay metrics, which are closed from delay equations that are very efficient and easy to implement. The response of the interconnect network is then represented as the sum of exponential functions. The Elmore delay [3] approximation is the most widely used delay model in the performance driven design of RC interconnect. However, Elmore delay can not accurately estimate the delay for RC interconnects lines [4].

The Elmore constant, or first moment of the impulse response has been, for a long time, the standard delay metric for interconnect performance driven design optimization. The mean value of delay is taken as an approximation to the time at which the output voltage of the interconnect v(t), for a step input, reaches 50% of its final value,

$$\tau_D = \int_0^\infty tv(t)dt$$

With decreasing rise times and minimum feature sizes, Elmore delay ceases to be the accurate metric for interconnect analysis and synthesis. It provides ovary pessimistic delay measure for RC circuit with general finite ramp inputs. Since interconnect resistance is higher, its shielding effect [5] is more important. Elmore delay, neglecting the resistance shielding, does not capture the correct sensitive, which is very crucial. This can lead to unacceptably large errors due to the fact that it tends to neglect the screening of the downstream capacitance of the interconnect by its resistance [6-7]. Alpert *et al.* [6] proposed two RC delay metrics which they claimed to be virtually as simple and as fast as the Elmore metric. Interconnect delay computation is critical tasks which may be executed millions of time during floor planning, placement and routing [8]. So efficient, highly accurate and closed from delay and slew metrics are very important for IC design. As such efficiency [11] of interconnect analysis is critical in a statistical timing flow, the advances in technology that result in scaled, multi level interconnect may address the wire ability problem but in the process create problem with signal

integrity and interconnect delay. A number of interconnect delay metrics are proposed recently with varying accuracy [9-15]. Most of these are based on the assumption that matching the first three moment of the impulse response result in a circuit that can describe the electrical behaviour of the linear RC line which models the interconnects accurately. In [9], the authors have proposed an explicit RC circuit delay model using the first three moments. In [10], the delay metric is based on comparing the impulse response to the h-gamma distribution. In [11], the gamma distribution is selected to model the normalized homogenous portion of the step response. While the Elmore delay is provably an upper bound for the 50% delay for large class of RC tree response, the tightness of the bound varies significantly from one node to create higher order (2-pole) moment matching models from which the delay can be approximated explicitly. The result is a delay metric in terms of the first three moment of the impulse response which provides accuracy similar to two pole models. These metrics are more accurate, thereby prohibiting the use of higher order Krylov space methods [12]. Asymptotic Waveform Evaluation (AWE) [13] is proposed with partial pade capability that produces provably stable two-pole models using the moments at the driven point and load end. In [14], a closed form expression for delay using first three circuit moments of the impulse response has been presented based on double pole approximation**.** In current mode signalling technique [15], an equivalent lumped element model can predict the step response of an interconnect line for both current and voltage mode signalling. The mean of an RC circuit can be calculated in a recursive way, and the resulting equivalent Elmore delay is in a simple closed form. However, what we really want to find is not the mean but the median of the distribution since it corresponds to the 50% delay point. Alpert et al. [6] proposed two RC delay metrics which they claimed to be virtually as simple and as fast as the Elmore metric. But significantly more accurate .One of these was the D3M (delay via three moment) metric after some process, they found that the following form of D3M consistently correlated best with the actual delay

$$D2M = \frac{M_1^2}{2\sqrt{M_2} - \left(\frac{M_3}{M_1}\right)} IN2$$

Elmore delay is proven to be the upper bound of the propagation delay [7]. In many cases, especially for the near end nodes, there is significant difference between the mean and the median of the impulse response waveform. Asymptotic Waveform Evaluation (AWE) [13], can approach towards HSPICE like accuracy by computing and matching higher order moments of the impulse response, but AWE does not provides any closed form formula, in particular it involves finding a solution of non linear equations. There are other different interconnect delay models proposed which are suitable for different frequency of operations [16-19].

In the following sections, we will explain the derivation of D3M metric at any arbitrary point on the interconnect line, with an accuracy of 50% compared to HSPICE simulation. And this paper next step (2) is devoted to the derivation of the metric for delays measured at the output interconnect.

The delay model proposed in this paper is suitable for moderate frequency range and hence RC interconnect is considered to derive the delay metric.

This paper is organized as follows: Section II discusses the proposed delay model for on-chip interconnects lines. Section III presents and discusses the simulation results. Finally section IV concludes the paper.

II. Proposed Delay Model

The proposed work is divided in two sub-sections. In the first sub-section, an analytical delay model for RC VLSI interconnect is proposed for the output node *out*; whereas, in the second sub-section, the analytical model is extended for an arbitrary point *int* in the interconnect.

A. Delay metric at 'out' node of the RC interconnect line

Let us consider the RC circuit as shown in Figure 1, which is a two stage RC model for estimation of the output response in an interconnect line.

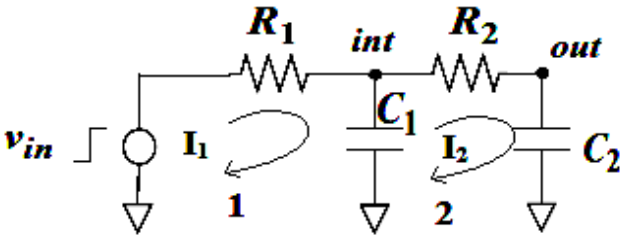

Figure 1. Two Stage RC Circuit

Kirchhoff's Voltage Law is applied in loop 1 and loop 2, respectively. For loop 1,

$$v_{in} - i_1 r_1 - \frac{(i_1 - i_2)}{c_1 s} = 0 \quad (1)$$

or, $$v_{in} = i_1\left(r_1 + \frac{1}{c_1 s}\right) - \frac{i_2}{sc_1} \quad (2)$$

For loop 2, $$\frac{i_1}{sc_1} - i_2\left[\frac{r_1 c_1 c_2 s + c_1 + c_2}{c_1 c_2 s}\right] = 0 \quad (3)$$

$$v_0 = \frac{i_2}{sc_2} \quad (4)$$

Solving (2) and (3) yields,

$$i_2 = \frac{v_{in} s c_2}{r_1 r_2 c_1 c_2 s^2 + [r_1 c_1 + (r_1 + r_2)c_2]s + 1} \quad (5)$$

Substituting the value of i_2 form (5) in (4) results in (6),

$$\frac{v_0}{v_{in}} = \frac{1}{r_1 r_2 c_1 c_2 s^2 + [r_1 c_1 + (r_1 + r_2)c_2]s + 1} \quad (6)$$

Let $h(t)$ be the time domain impulse response of the RC circuit. The corresponding transfer function $h(s)$ is expressed in term of RC interconnects' parameters,

$$h(s) = \frac{1}{r_1 r_2 c_1 c_2 s^2 + [r_1 c_1 + (r_1 + r_2)c_2]s + 1} \quad (7)$$

Consider a transfer function $h(s)$ of the RC circuit, and assume that a sufficient number of its moments is calculated form the circuit,

$$h(s) = \frac{1}{1 + a_1 s + a_2 s^2} = 1 + m_1 s + m_2 s^2 \quad (8)$$

The first three moments of the transfer function can be expressed easily in term of resistance and capacitances,

$$m_1 = -\left[r_1c_1 + (r_1 + r_2)c_2\right] \quad (9)$$

$$m_2 = -\left[r_1r_2c_1c_2 - \left[r_1c_1 + (r_1 + r_2)c_2\right]^2\right] \quad (10)$$

$$m_3 = \left[r_1c_1 + (r_1 + r_2)c_2\right]\left[2r_1c_1r_2c_2 - (r_1c_1 + (r_1 + r_2)c_2)^2\right] \quad (11)$$

The transfer function $h(s)$ can be expressed in term of its moments [13],

$$h(s) = \frac{1}{\left[m_2 - \frac{m_3}{m_1}\right]s^2 - m_1 s + 1} \quad (12)$$

Hence, its poles in terms of first three moments are sufficient to describe the transfer function. The stable two poles (S2P) approximation consists of transfer function h(s) and the poles are found form the driving point moments; hence its poles are given as:

$$p_{1,2} = \frac{m_1 \pm \sqrt{m_1^2 - 4\left[m_2 - \left(\frac{m_3}{m_1}\right)\right]}}{2\left[m_2 - \left(\frac{m_3}{m_1}\right)\right]} \quad (13)$$

Two extreme cases are discussed here regarding the relationships between two poles, i.e. dominant and coincident poles.

1) Dominant pole

Here both poles are real and $p_1 >> p_2$; also it can describe the 50% delay,

$$m_1 >> 2\sqrt{m_2 - \left[\frac{m_3}{m_1}\right]} \quad (14)$$

Therefore, D3M delay metric proposed in [6] is,

$$t_{d0.5} = -\frac{1}{p_1}\ln 2 = -m_1 \ln 2 \quad (15)$$

The model proposed in [6] is referred to as the scaled Elmore delay in term of first three moments. Therefore, in this particular case (15) can also be expressed as,

$$t_{d0.5} = 0.5\frac{m_1^2}{\sqrt{m_2 - \left[\frac{m_3}{m_1}\right]}} \quad (16)$$

This shows that Delay Metric with three moments (D3M) is a special case.

2) Coincident pole

In this condition both poles are equal i.e. $p_1 = p_2$. This occurs when the discriminator in (13) is zero. Therefore, from (13) we have,

$$m_1 = 4\left[m_2 - \left[\frac{m_3}{m_1}\right]\right] \quad (17)$$

Hence the double pole p of the transfer function can be expressed in term of first three moments as,

$$p = 4\left(\frac{\sqrt{m_2 - \frac{m_3}{m_1}}}{m_1^2}\right) \quad (18)$$

So, the transfer function of the RC circuit for step response at node *out* is,

$$\frac{v_{out}}{v_{in}} = \frac{1}{r_1r_2c_1c_2s^2 + \left[r_1c_1 + (r_1 + r_2)c_2\right]s + 1} = \frac{1}{((s-p)^2)}$$

In the case of step response,

$$v_{in} = \frac{v_0}{s}$$

Therefore, $v_{out}(s) = \frac{v_o}{s(s-p)^2}$

or, $v_{out}(s) = v_o\left[\frac{k_1}{s} + \frac{k_2}{(s-p)} + \frac{k_3}{(s-p)^2}\right]$

So, $v_{out}(s) = v_o\left[\frac{1}{s} - \frac{1}{(s-p)} - \frac{p}{(s-p)^2}\right]$ (19)

Taking inverse Laplace transform of (19), we get,

$$v_{out}(t) = 1 - e^{pt} - pte^{pt} \quad (20)$$

Here, unlike [6], an equivalent pole is not approximated. Rather, in this derivation, desired delay would be computed from the behaviour of the waveform described by (20). To compute the equivalent single pole p_{eq} that yields the same 50% delay for the circuit, we solve (20) using (15) with p replaced by p_{eq},

$$v_{out}(t_{d0.5}) = 1 - e^{p\left(-\frac{1}{p_{eq}}in2\right)} - p\left(-\frac{1}{p_{eq}}in2\right)e^{p\left(-\frac{1}{p_{eq}}in2\right)} = 0.5 \quad (21)$$

Solving (21) yields the value of $\frac{p_{eq}}{p}$,

$$\frac{p_{eq}}{p} \approx 0.413$$

so $p_{eq} = -1.75\left[\sqrt{m_2 - \left(\frac{m_3}{m_1}\right)}\Big/ m_1^2\right]$ (22)

Hence, solving (22), we get 50% delay for coincident poles and is given by,

$$t_{d0.5} = 0.571\left(\frac{m_1^2}{\sqrt{m_2 - \left(\frac{m_3}{m_1}\right)}}\right) \quad (23)$$

Therefore, comparing (16) and (23) one gets that 50% delay for these two extreme cases differs by a factor. Therefore, one can assume that in general case, for an arbitrary ratio $m_1^2\Big/\sqrt{m_2 - \frac{m_3}{m_1}}$ and, there is a factor $\delta^{(0.5)}$ such that the 50% delay point of the step response of a two pole circuit can be expressed in the form given in (24),

$$t_{0.5} = \delta^{(0.5)}\frac{m_1^2}{\sqrt{m_2 - \left[\frac{m_3}{m_1}\right]}}\ln 2 \quad (24)$$

where $0.571 \le \delta^{(0.5)} \le 0.5$ (25)

i.e., $\frac{1}{1.75} \le \delta^{(0.5)} \le \frac{1}{2}$ (26)

Equation (24) represents the required expression for 50% delay for the output node. A similar procedure can be

adopted to compute the 70% delay point at the output of the circuit in Figure 1. This leads to the following result:

$$t_{d0.7} = \delta^{(0.7)}.\frac{m_1^2}{\sqrt{m_2 - \frac{m_3}{m_1}}} \quad (27)$$

Similarly the 70% delay point of the step response of a 2-pole circuit for the dominant poles can be expressed in the form as given in (28),

$$t_{d0.7} = 0.57\left(\frac{m_1^2}{\sqrt{m_2 - \frac{m_3}{m_1}}}\right) \quad (28)$$

Same procedure can be used for the case of coincident poles; hence 70% delay for the coincident poles is given by,

$$t_{d0.7} = 0.663\left[\frac{m_1^2}{\sqrt{m_2 - \frac{m_3}{m_1}}}\right] \quad (29)$$

Comparing (28) and (29), 70% delay of the step response,

$$t_{d0.7} \le \delta^{(0.7)} \le \frac{m_1^2}{\sqrt{m_2 - \frac{m_3}{m_1}}} \ln 3.33 \quad (30)$$

Therefore, $0.663 \le \delta^{(0.7)} \le 0.57$ (31)

Note that, in comparison to the 50% delay metric, the error resulting from using some average value based on (31) for $t_{d0.7}$ is greater.

B. Derivation of the delay metric at an arbitrary point in RC interconnect line

As seen in the previous sub section, the delay metric given by (24) and (27) is quite stable delay metric for nodes at the far end of an interconnect line i.e., the associated correction factor δ does not span for a large value; therefore, using an average value (average of a practical range of $\left(m_1^2\right)\Big/\left(\sqrt{m_2 - \frac{m_3}{m_1}}\right)$ is sufficient. However, as already discussed in [6], such a metric is not suitable for near end nodes. Let us consider the RC circuit in figure 1.which can be two stage RC model for the out response of an interconnect line. Hence we calculated the transfer function at the intermediate node *int* of the circuit.

Now KVL is applied in the circuit model shown in Figure 1.For loop 1,

$$v_{in} - i_1 r_1 - \frac{(i_1 - i_2)}{c_1 s} = 0 \quad (32)$$

$$v_{in} = i_1\left(r_1 + \frac{1}{c_1 s}\right) - \frac{i_2}{s c_1} \quad (33)$$

For loop 2,

$$\frac{i_1}{s c_1} - i_2\left[\frac{r_1 c_1 c_2 s + c_1 + c_2}{c_1 c_2 s}\right] = 0 \quad (34)$$

$$v_0 = \frac{i_1}{s c_1} \quad (35)$$

Solving (33) and (34), we get,

$$i_1 = \frac{v_{in}(r_2 c_2 s + 1) s c_1}{r_1 r_2 c_1 c_2 s^2 + [r_1 c_1 + (r_1 + r_2) c_2] s + 1} \quad (36)$$

Substituting the value of i_1 from (36) in (35) yields,

$$\frac{v_{out}}{v_{in}} = \frac{(r_2 c_2 s + 1)}{r_1 r_2 c_1 c_2 s^2 + [r_1 c_1 + (r_1 + r_2) c_2] s + 1}$$

Thus, the transfer function at the intermediate node is,

$$h(s) = \frac{v_{out}}{v_{in}} = \frac{r_2 c_2 s + 1}{r_1 r_2 c_1 c_2 s^2 + [r_1 c_1 + (r_1 + r_2) c_2] s + 1} \quad (37)$$

The transfer function can be expressed as a ratio of two polynomials. Assume that a sufficient number of moments are calculated from the circuit,

$$h(s) = \frac{1 + b_1 s}{1 + a_1 s + a_2 s^2} = 1 + m_1 s + m_2 s^2 \quad (38)$$

The first three moments of the transfer function can be expressed easily in term of resistance and capacitance values,

$$m_1 = -r_1(c_1 + c_2)$$

$$m_2 = [r_1(c_1 + c_2)]^2 + r_1 r_2 c_2^2$$

$$m_3 = r_1^2 r_2 c_1^2 c_2 - r_1(c_1 + c_2)\,[r_1 c_1 + (r_1 + r_2) c_2] - r_1 r_2 c_2^2 (r_1 + r_2)$$

From the above three equations, the coefficients of denominator polynomials may be expressed as,

$$\left.\begin{aligned} a_1 &= \frac{m_1 m_2 - m_3}{m_2 - m_1^2}; \\ a_2 &= \frac{m_1 m_3 - m_2^2}{m_2 - m_1^2} \end{aligned}\right\} \quad (39)$$

refers to as two poles approximate with explicit moment matching The transfer function of the circuit can be expressed in term of its moments [8] as,

$$h(s) = \frac{m_2 - m_1^2 + (2 m_1 m_2 - m_3 - m_1^3)}{m_2 - m_1^2 + (m_1 m_2 - m_3) s + (m_1 m_3 - m_2^2) s^2} \quad (40)$$

Since the first three moments are sufficient to describe the Transfer function of such a circuit, a delay metric that takes only these three moments into account should be sufficient. The poles of this circuit are then:

$$\left.\begin{aligned} p_1 &= \frac{-(m_1 m_2 - m_3) + \sqrt{(m_1 m_2 - m_3)^2 - 4(m_1 m_3 - m_2^2)(m_2 - m_1^2)}}{2(m_1 m_3 - m_2^2)} \\ p_2 &= \frac{-(m_1 m_2 - m_3) - \sqrt{(m_1 m_2 - m_3)^2 - 4(m_1 m_3 - m_2^2)(m_2 - m_1^2)}}{2(m_1 m_3 - m_2^2)} \end{aligned}\right\} \quad (41)$$

As also done in the previous sub section, let us examine the two extreme cases in the relationship between the two poles,

1) Dominant pole

We know that in case of dominant pole $P_1 >> P_2$ (both are real and negative),

$$m_3^2 >> 3(m_1^2 m_2^2 + 2 m_1 m_2 m_3) \quad (42)$$

Therefore its 50% delay for a step input can be given as,

$$t_{d0.5} = -\frac{1}{p_2} \ln 2 = -m_3 \ln 2 \quad (43)$$

or, $t_{d0.5} = \frac{1}{\sqrt{3}} \frac{m_3^2}{\sqrt{m_1 m_2 (m_1 m_2 + 2m_3)}}$ (44)

This equation is the D3M delay metric [4].

2) Coincident pole

This is similar to the previous section where $P_1=P_2$. This occurs when the discriminator in (41) is nil. Therefore, from (41) we have,

$$(m_1 m_2 - m_3)^2 = 4[m_1 m_2 (m_1 m_2 + m_3)] \quad (45)$$

Hence, the doubles pole p of the transfer function can be expressed in term of first three moments as,

$$p = 4 \frac{\sqrt{m_1 m_2 (m_1 m_2 + m_3)}}{m_3^2} \quad (46)$$

In this case, the step response of the circuit at any arbitrary point is,

$$\frac{v_{out}}{v_{in}} = \frac{1 + r_2 c_2 s}{r_1 r_2 c_1 c_2 s + [r_1 c_1 + (r_1 + r_2)s + 1]} = \frac{1}{(s - p^2)}$$

In the case of step response,

$$v_{in} = \frac{v_0}{s}$$

Therefore,

$$v_{out} = \frac{v_o}{s(s-p)^2}$$

$$v_{out} = v_o \left[\frac{k_1}{s} + \frac{k_2}{(s-p)} + \frac{k_3}{(s-p)^2} \right]$$

$$v_{out} = v_o \left[\frac{1}{s} - \frac{1}{(s-p)} - \frac{p(pr_2c_2 + 1)}{(s-p)^2} \right] \quad (47)$$

And taking inverse Laplace transform of (47), we get,

$$v_{out}(t) = 1 - e^{pt} - p(pr_2c_2 + 1)te^{pt} \quad (48)$$

Here, unlike [6], we do not consider an equivalent pole that captures, approximately, the behaviour of the entire waveform described by (48), from which the desired delay point would be computed. The reason is that a two time constant behaviour can be approximated using a single pole unless one of the times constant is negligible with respect to the other. To compute the equivalent single pole p_{eq} that yields the same 50% delay for the circuit, we solve (48) using (43) with p replaced by p_{eq},

$$v_{out}(t_{d0.5}) = 1 - e^{p\left(-\frac{1}{p_{eq}} in 2\right)} - p(pr_2c_2 + 1)\left(-\frac{1}{p_{eq}} \ln 2\right) e^{p\left(-\frac{1}{p_{eq}} in 2\right)} = 0.5 \quad (49)$$

Hence, a numerical solution of this equation yields the following value of the ratio p/p_{eq},

$$\frac{p_{eq}}{p} \approx 0.413 \Rightarrow p_{eq} = -1.752 \left[\frac{\sqrt{m_2 m_2 (m_1 m_2 + m_3)}}{m_3^2} \right] \quad (50)$$

Hence, solving this equation, we get the 50% delay for coincident pole and is given by,

$$t_{0.5} = 0.570 \left[\frac{m_3^2}{m_1 m_2 (m_1 m_2 + m_3)} \right] \quad (51)$$

Therefore, comparing (45) and (51), we get that 50% for these two extreme cases differs by a factor. Therefore one can assume that in general case, there is a factor $\delta^{(0.5)}$ such that the 50% delay point of the step response of a 2- pole circuit can be expressed in the form,

$$t_{0.5} = \delta^{(0.5)} \frac{m_3^2}{\sqrt{m_2 m_1 (m_1 m_2 + m_3)}} \ln 2 \quad (52)$$

where

$$0.570 \le \delta^{(0.5)} \le 0.577 \quad (53)$$

Equation (52) represents the required expression for 50% delay for the arbitrary node.

Following the similar steps, we get the 70% delay point at that output node of the RC interconnect,

$$t_{d0.7} = \delta^{(0.7)} \frac{m_1^2}{\sqrt{m_2 - \frac{m_3}{m_1}}} \quad (54)$$

Therefore, in case of step response 70% delay for the dominant poles is given as,

$$t_{d0.7} = 0.596 \left[\frac{m_3^2}{\sqrt{m_1 m_2 (m_1 m_2 + m_3)}} \right] \quad (55)$$

Same procedure can be used for the case of coincident pole; hence, 70% delay for the coincident poles is given by,

$$t_{d0.7} = 0.600 \left[\frac{m_3^2}{\sqrt{m_1 m_2 (m_1 m_2 + m_3)}} \right] \quad (56)$$

Comparing (54) and (55), 70% delay of the step response is,

$$t_{d0.7} \le \delta^{(0.7)} \le \frac{m_3^2}{\sqrt{m_2 m_1 (m_1 m_2 + m_3)}} \ln 3.33 \quad (57)$$

Therefore,

$$0.0596 \le \delta^{(0.7)} \le 0.600 \quad (58)$$

It can be observed that in comparison to the 50% delay metric, the error resulting from using some average value based on (58) for $t_{d0.7}$ is greater.

Again, we study two extreme cases corresponding to the relative importance of the zero at node *int* in Figure 1, from which a general delay model is deduced for higher order RC interconnect models. It is assumed, without loss of generality, that the position of the zero in the frequency is determined with respect to R_2.

1. ***Low frequency zero***: This corresponds to a very large value of R_2 which causes the zero to move down in frequency partially cancelling the effect of the poles. This also means that R_2 "screens" a large portion of C_2 from node *int*. In the case where $R_2 \rightarrow \infty$, the 50% delay reduce to,

$$t_{d0.5} = \left(\frac{m_3^2}{\sqrt{m_1 m_2 (m_1 m_2 + m_3)}} \right)_{\text{int}, ind} \ln 2 \quad (59)$$

Here, the index *int* indicates that the moments are those associated with the node of the same name, the second index (for independent) means that only the circuit upstream of node *int* is taken into account, i.e. the circuit section (R_1C_1).

2. ***High frequency zero***: This corresponds to the situation where R_2 is very small. In this case where $R_2 \rightarrow 0$, the

screening effect is nil and the delay at node *int* coincides to the delay at the far end node (*out*); thus we can write;

$$t_{d0.5} = \left(\frac{m_1^2}{\sqrt{m_2 - \frac{m_3}{m_1}}} \right)_{out} \ln 2 \quad (60)$$

Now note that the expression of the delay in (49) can be written in term of the delay expressed in (59).Considering the benchmark circuit shown in Figure 1,

$$t_{d0.5} = \left(\left(\frac{m_3^2}{\sqrt{m_1 m_2 (m_1 m_2 + m_3)}} \right)_{int-ind} + r_1 c_2 \right) \ln 2 \quad (61)$$

For higher order RC interconnect circuit, the time constant R_1C_2 constant can be shown to be the sum of the all capacitance downstream of the node of interest (*int*), C_{dint} multiplied by the discharge resistive path (to the source) upstream of *int*, $r_{Uint.}$ Therefore, a more general expression (for higher order circuit) is,

$$t_{d0.5} = \left(\left(\frac{m_3^2}{\sqrt{m_1 m_2 (m_1 m_2 + m_3)}} \right)_{int-ind} + r_{U\,\mathrm{int}} c_{d\,\mathrm{int}} \right) \ln 2 \quad (62)$$

For the general case where a portion of C_{dint} is screened, the delay at an intermediate node can be (intuitively) expressed; where B is a parameter that quantifies the screening effect although the derivation of B is beyond the scope of this paper, one can easily develop an intuitive understanding of such a parameter. A classical approach consists of simply taking B as an exponential function of the ratio of the first moments at node *int* and *out*. The problem with this approach is that first moments are inherently inappropriate to model signal transitions on which the screening effect is strongly dependent [7], therefore a formulation of B that take in to account the second and third moments is more appropriate, in our case B is expressed is follow;

$$B = \left(\left(\frac{m_3^2}{\sqrt{m_1 m_2 (m_1 m_2 + m_3)}} \right)_{\mathrm{int}} \Big/ \left(\frac{m_1^2}{\sqrt{m_2 - \frac{m_3}{m_1}}} \right)_{\mathrm{out}} \right) \quad (63)$$

III. Experimental Results

The comparative result of the proposed models for output node as well as arbitrary node int with SPICE delay and Elmore delay for the different values of C is illustrated in Tables 1-4. From the tables, it is evident that the proposed delay models for both cases results in an error of as low as 10% when compared with that of SPICE simulations. Figures 2-4 show the graphical comparisons in among SPICE 50 % delay, Equivalent Elmore 50 % delay and the proposed 50 % delay model for the different values of load capacitances. From the graphs we can analyse that the behaviour of the proposed delay model for 50% is similar to that of the SPICE and Equivalent Elmore delay models. From the figures it is observed that as the value of the load capacitance increased, the delay in the nets also increases and it is least in the low frequency for the arbitrary point node int on the interconnect line.

Graphical comparisons of the % error in between SPICE with Elmore model and SPICE with proposed model for 50 % delay model for different values of load capacitances are drawn in Figures 5-7. From all the figures we can analyse that the proposed delay model for 50 % threshold shows better accuracy and efficiency that equivalent Elmore delay. From the simulation results we can also analyse that our proposed model has less error comparable to equivalent Elmore model and it is found to be within 10 % of the SPICE values.

C (pF)	SPICE 50 % Delay for int T_{int} (µs)	Equivalent Elmore model 50 % Delay	% Error	Proposed model for 50 % delay	% Error
240	35	31	11.42	37	5.74
290	41	38	7.31	44	7.31
340	52	47	9.61	54	3.84
390	61	54	11.4	67	9.83
440	68	61	10.29	72	5.88

Table 1. Comparison between Elmore and the proposed delay with spice result for low frequency for 'int' node.

C (pF)	SPICE 50 % Delay for int T_{int} (µs)	Equivalent Elmore model 50 % Delay	% Error	Proposed model for 50 % delay	% Error
240	56	45	19.6	44	3.57
290	68	54	20.58	58	7.34
340	75	63	16.01	66	8.01
390	91	76	16.48	79	3.29
440	98	81	17.34	82	3.06

Table 2. Comparison Between Elmore and the Proposed Delay with Spice Result For High Frequency For 'int' Node.

C (pF)	SPICE 50 % Delay for int T_{int} (µs)	Equivalent Elmore model 50 % Delay	% Error	Proposed model for 50 % delay	% Error
240	43	39	9.31	54	2.32
290	57	51	10.52	63	1.75
340	63	57	9.52	69	4.17
390	74	63	14.84	88	6.75
440	79	70	11.39	95	3.79

Table 3. Comparison Between Elmore and the Proposed Delay with Spice Result for Dominant for Out Node.

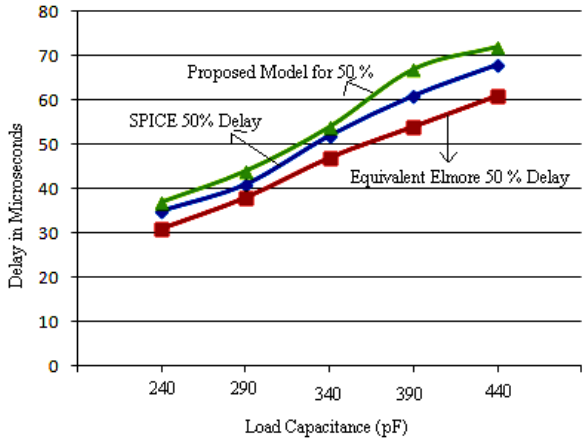

Figure 2. Comparison between Elmore and the Proposed Delay with SPICE result for Low Frequency for Int Node

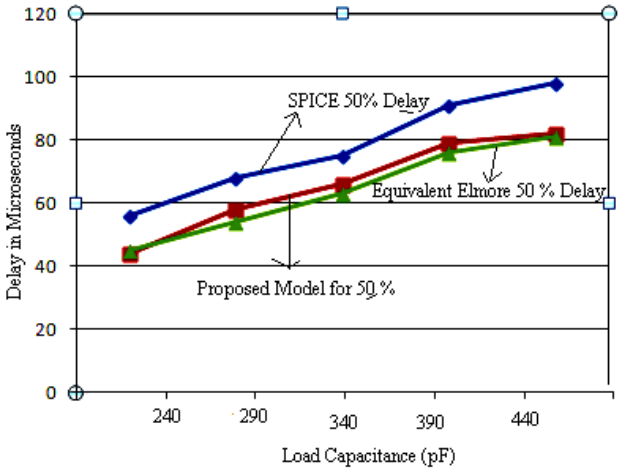

Figure 3. Comparison between Elmore and the Proposed Delay with SPICE result for High Frequency for Int Node

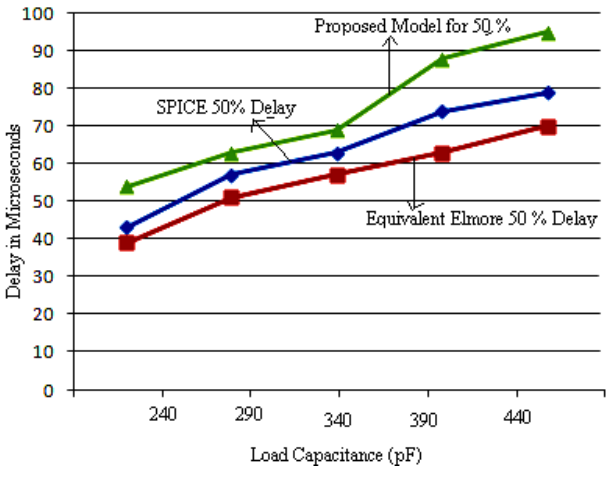

Figure 4. Comparison between Elmore and the Proposed Delay with SPICE result for Dominant Pole for Out Node

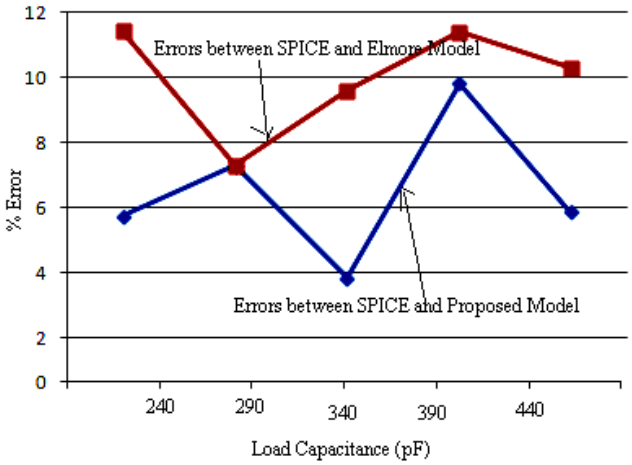

Figure 5. Comparison of % Errors between Elmore and the Proposed Delay with SPICE result for Low Frequency for Int Node

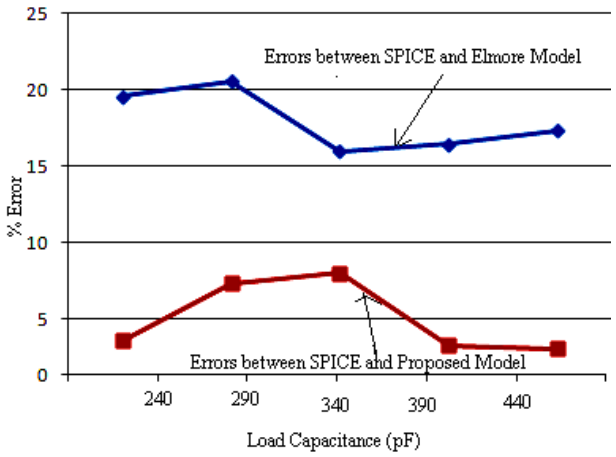

Figure 6. Comparison of % Errors between Elmore and the Proposed Delay with SPICE result for High Frequency for Int Node

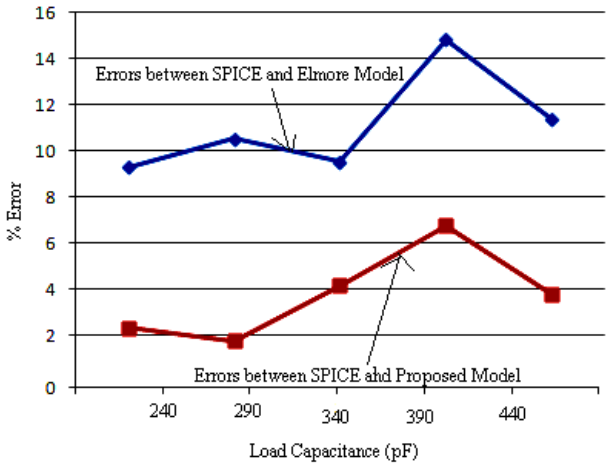

Figure 7. Comparison of % Error between Elmore and the Proposed Delay with SPICE result for Dominant Pole for Out Node

Figure 8 shows two RC response waveforms and their SPM (Single Pole) and DPM (Double Pole) approximations. It is clear from Figure 2 that in the cases of single pole and double pole, waveforms deviate significantly from a one-pole

exponential; however, in both the cases the 10-90% delay is modelled accurately by SPM and 50% delay is modelled well by DPM. Though neither SPM nor DPM match the complete output waveform shape, together they can capture the key delay points needed for timing analysis. It may also seem that approximating step response with one pole can cause a large error in delay estimation because the actual response can deviate significantly from a single pole exponential approximation.

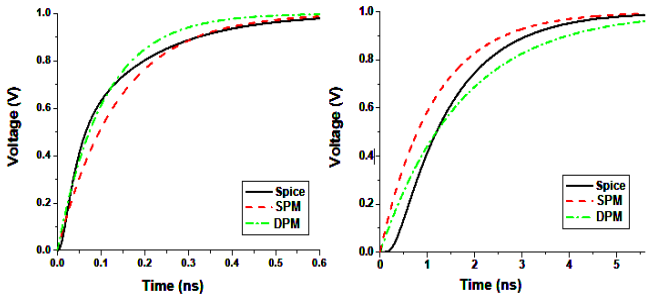

Figure 8. Comparison in SPICE, Single Pole Delay and Double Pole Delay Approximation

IV. Conclusion

Interconnect now dominates a number of design metrics. Various interconnect models have been presented over the last several decades. In this work, an accurate delay metric for resistive interconnect is presented, that computes the delay at any arbitrary point on the waveform and at any point along the interconnect. It is based on the first three moments of the impulse response. Two pole RC model is developed based on first, second and third moment effect for the delay estimation for interconnect lines. Proposed model is applicable to any type of interconnect line as this approach is not based on the analogy of the impulse response to a particular Probability Distribution Function (PDF). The SPICE simulation justifies the efficacy of the proposed delay modelling approach.

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